

P-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD25401Q3](#)

FEATURES

- Ultra Low Q_g and Q_{gd}
- Low Thermal Resistance
- Low $R_{DS(on)}$
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

APPLICATIONS

- DC-DC Converters
- Battery Management
- Load Switch
- Battery Protection

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion load management applications. The SON 3×3 package offers excellent thermal performance for the size of the package.

Table 1. PRODUCT SUMMARY

V _{DS}	Drain to Source Voltage	–20		V
Q _g	Gate Charge Total (4.5V)	8.8		nC
Q _{gd}	Gate Charge Gate to Drain	2.1		nC
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = –2.5V	13.5	mΩ
		V _{GS} = –4.5V	8.8	mΩ
V _{th}	Threshold Voltage	–0.85		V

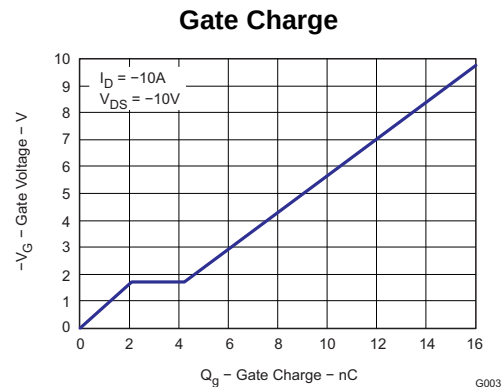
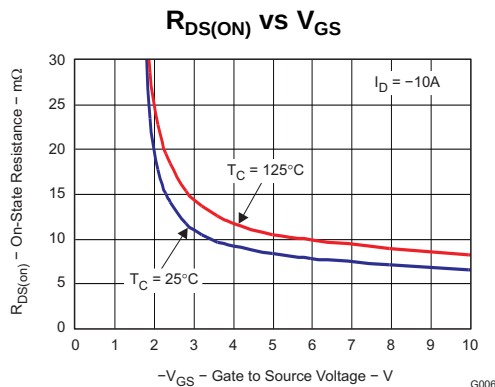
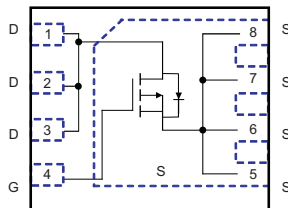
ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD25401Q3	SON 3 × 3 Plastic Package	13-inch reel	2500	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	–20	V
V_{GS}	Gate to Source Voltage	+12 / –12	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	–60	A
	Continuous Drain Current ⁽¹⁾	–14	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	–82	A
P_D	Power Dissipation ⁽¹⁾	2.8	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	$^\circ\text{C}$

- (1) $R_{\theta JA} = 45^\circ\text{C/W}$ on 1inch² Cu (2 oz.) on 0.060" thick FR4 PCB.
 (2) Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

Figure 1. Top View


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ELECTRICAL CHARACTERISTICS

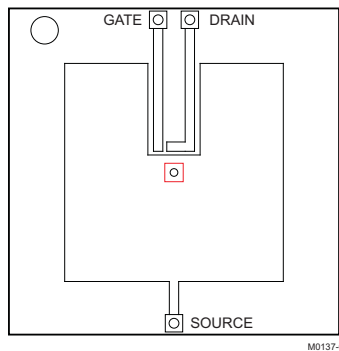
(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = −250μA	−20			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = −20V to −16V			−1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = ±12V			−100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = −250μA	−0.6	−0.85	−1.2	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = −2.5V, I _D = −10A		13.5	18.2	mΩ
		V _{GS} = −4.5V, I _D = −10A		8.8	11.7	mΩ
g _{fs}	Transconductance	V _{DS} = −15V, I _D = −10A		43		S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = −10V, f = 1MHz		1070	1400	pF
C _{OSS}	Output Capacitance			560	730	pF
C _{RSS}	Reverse Transfer Capacitance			180	230	pF
Q _g	Gate Charge Total (4.5V)	V _{DS} = −10V, I _D = −10A		8.8	12.3	nC
Q _{gd}	Gate Charge Gate to Drain			2.1		nC
Q _{gs}	Gate Charge Gate to Source			2.1		nC
Q _{g(th)}	Gate Charge at V _{th}			0.9		nC
Q _{OSS}	Output Charge	V _{DS} = −10V, V _{GS} = 0V		8.2		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = −10V, V _{GS} = −4.5V, I _D = −10A , R _G = 5.1Ω		8.1		ns
t _r	Rise Time			3.9		ns
t _{d(off)}	Turn Off Delay Time			13.5		ns
t _f	Fall Time			12.6		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _S = −10A, V _{GS} = 0V		−0.7	−1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = −12.5V, I _F = −10A, di/dt = 300A/μs		17.4		nC
t _{rr}	Reverse Recovery Time			21		ns

THERMAL INFORMATION

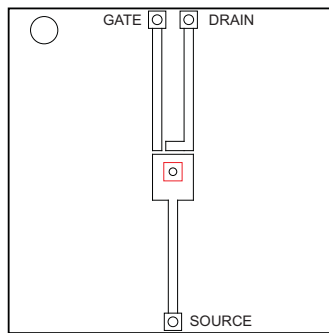
THERMAL METRIC ⁽¹⁾⁽²⁾		CSD25401Q3	UNITS
		8 PIN	
θ _{JA}	Junction-to-ambient thermal resistance	42.0	°C/W
θ _{JCTop}	Junction-to-case (top) thermal resistance	20.6	
θ _{JB}	Junction-to-board thermal resistance	8.8	
ψ _{JT}	Junction-to-top characterization parameter	0.3	
ψ _{JB}	Junction-to-board characterization parameter	8.7	
θ _{JCbot}	Junction-to-case (bottom) thermal resistance	0.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).(2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).



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Max $R_{\theta JA} = 57^{\circ}\text{C/W}$
when mounted on
1inch² of 2 oz. Cu.

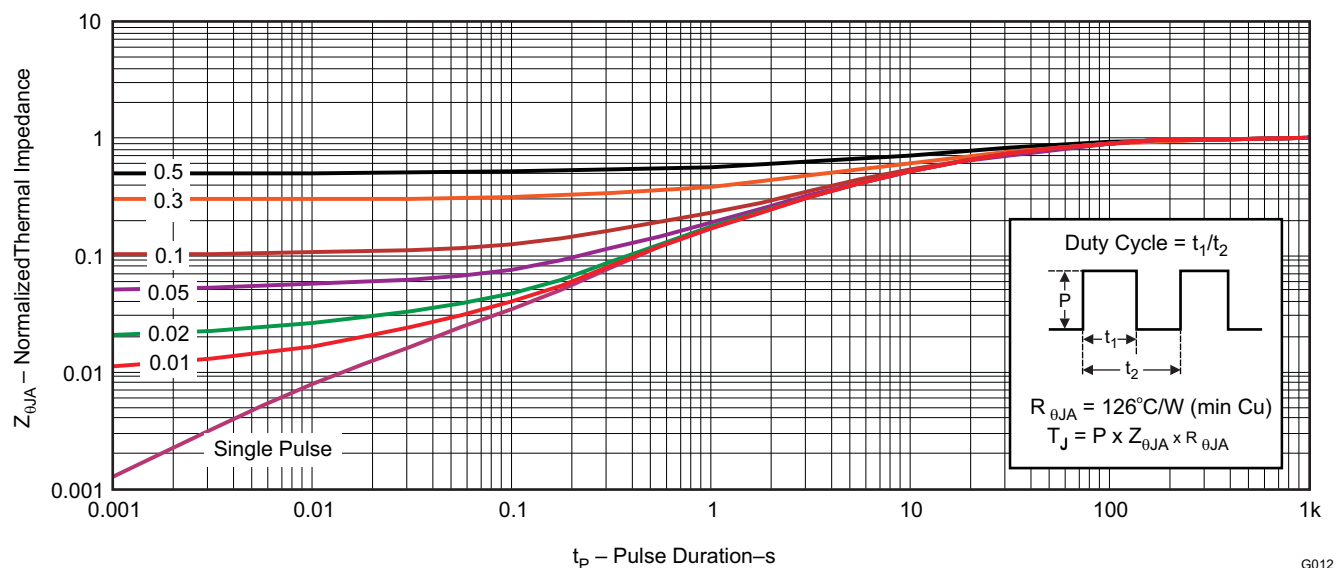


M0137-02

Max $R_{\theta JA} = 158^{\circ}\text{C/W}$
when mounted on
minimum pad area of 2
oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

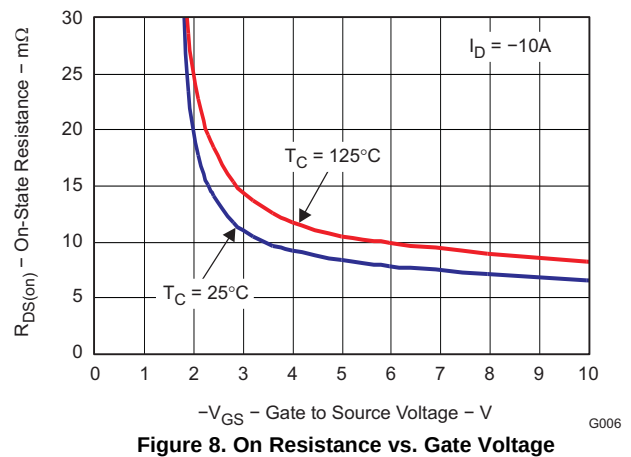
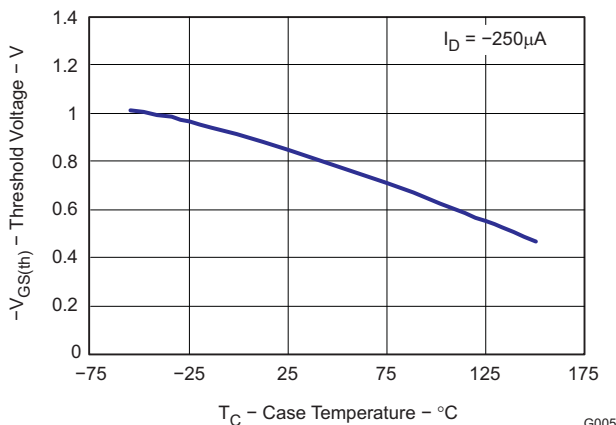
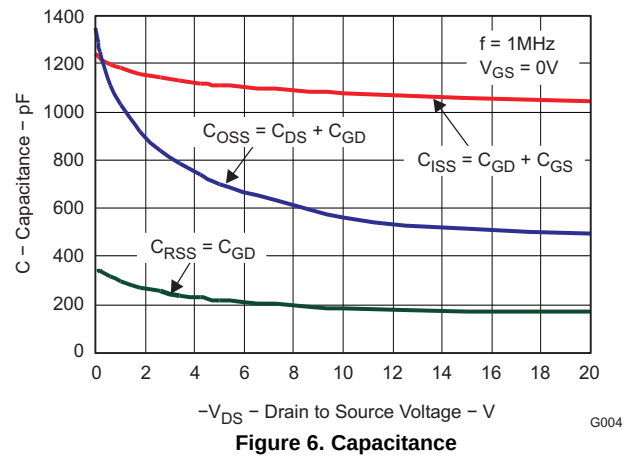
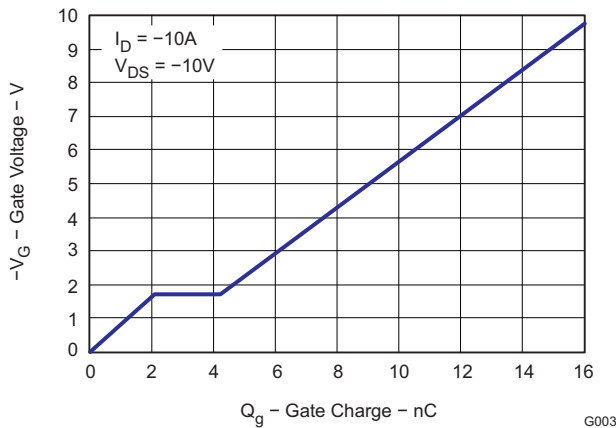
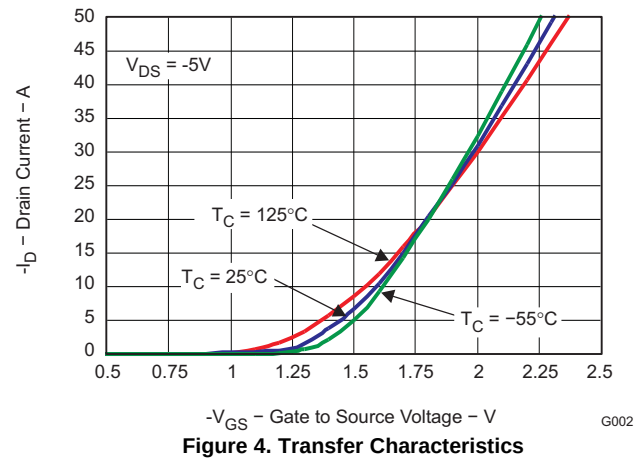
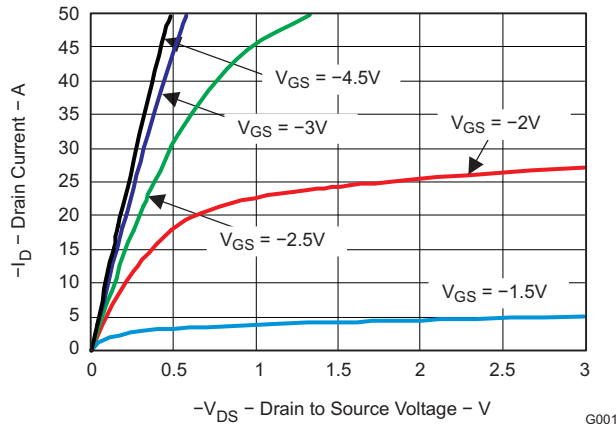


G012

Figure 2. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

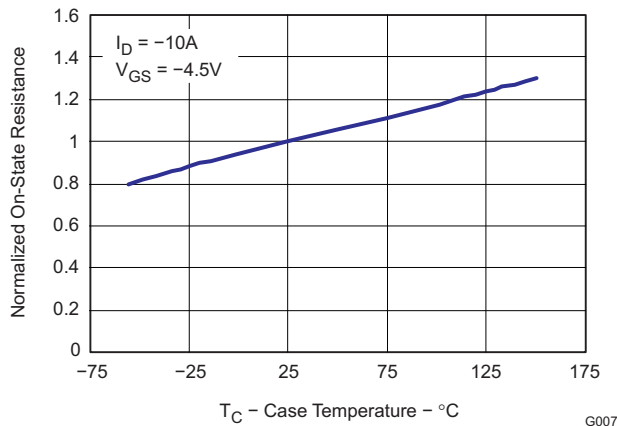


Figure 9. On Resistance vs. Temperature

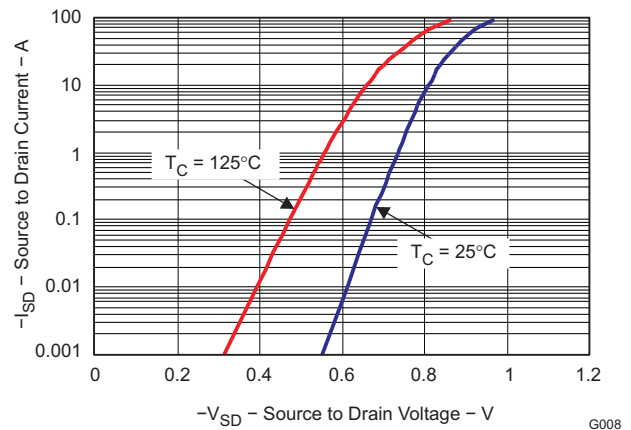


Figure 10. Typical Diode Forward Voltage

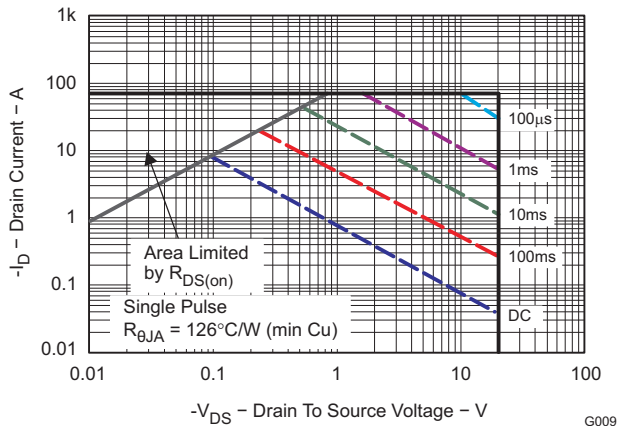


Figure 11. Maximum Safe Operating Area

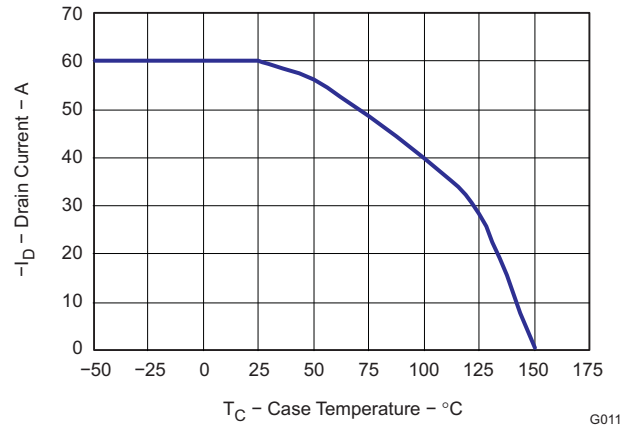
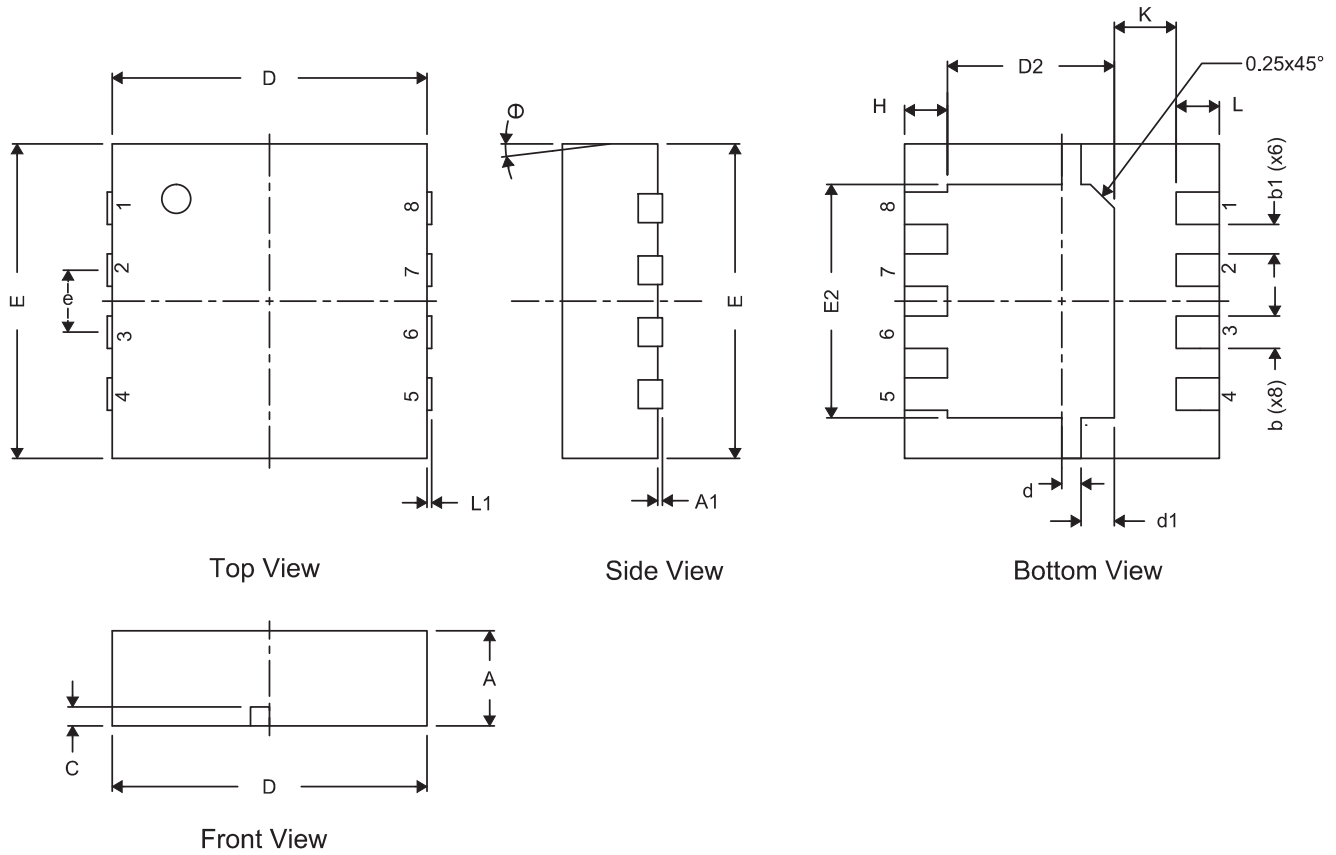
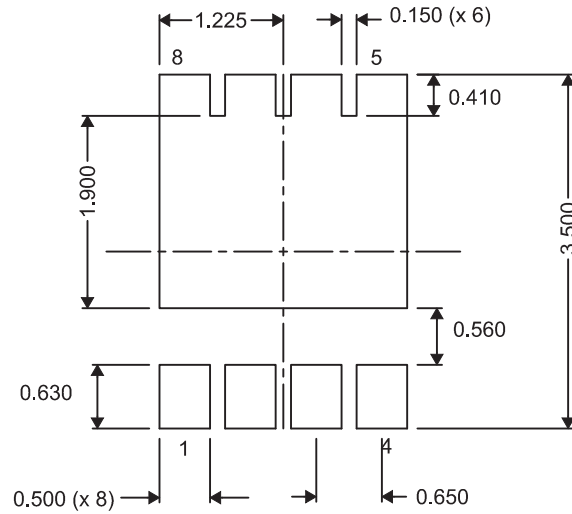


Figure 12. Maximum Drain Current vs. Temperature

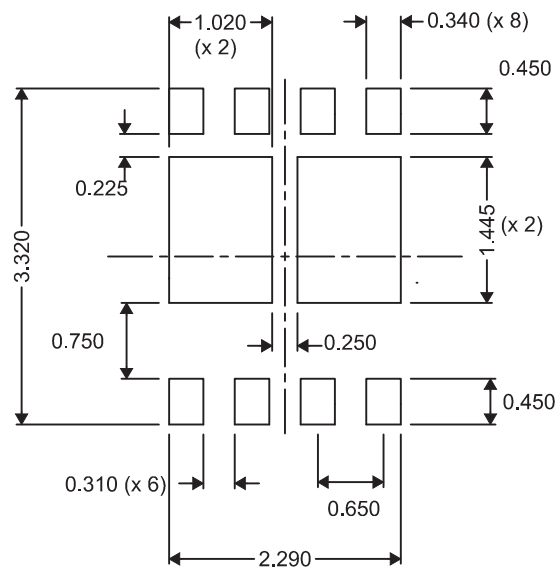
MECHANICAL DATA**CSD25401Q3 Package Dimensions**

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
b1	0.310 NOM			0.012 NOM		
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
d	0.150	0.200	0.250	0.006	0.008	0.010
d1	0.300	0.350	0.400	0.012	0.014	0.016
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026 TYP		
H	0.35	0.450	0.550	0.014	0.018	0.022
K	0.650 TYP			0.026 TYP		
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	0		0	0		0
θ	0		0	0		0

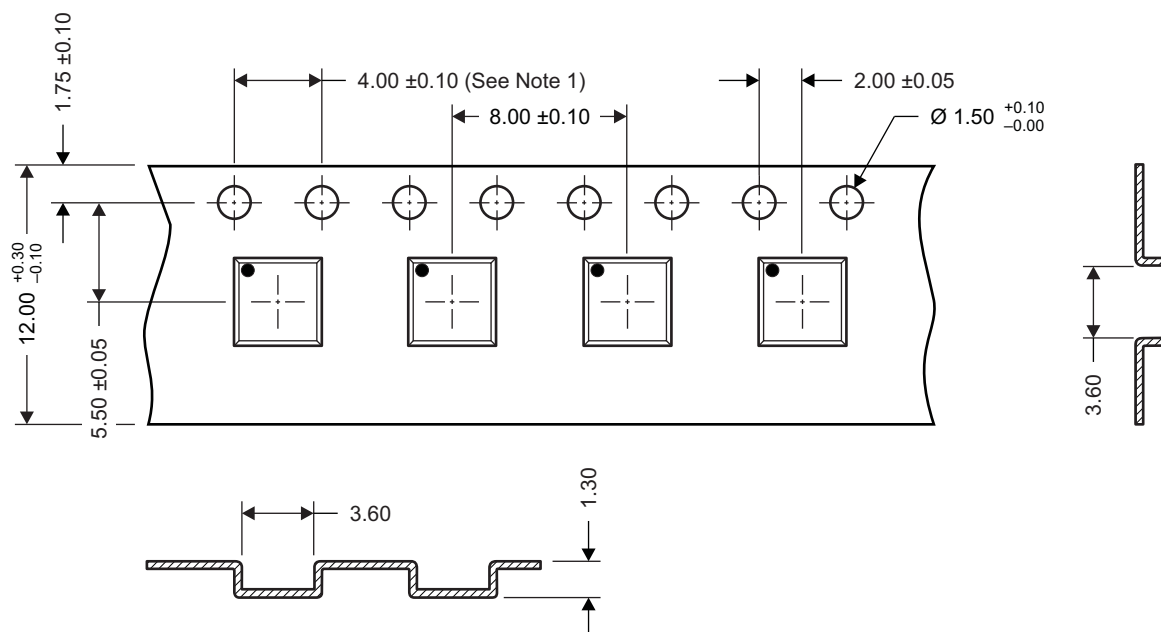
Recommended PCB Pattern



Recommended Stencil Opening



Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Conection) PbF Reflow Compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A **Page**

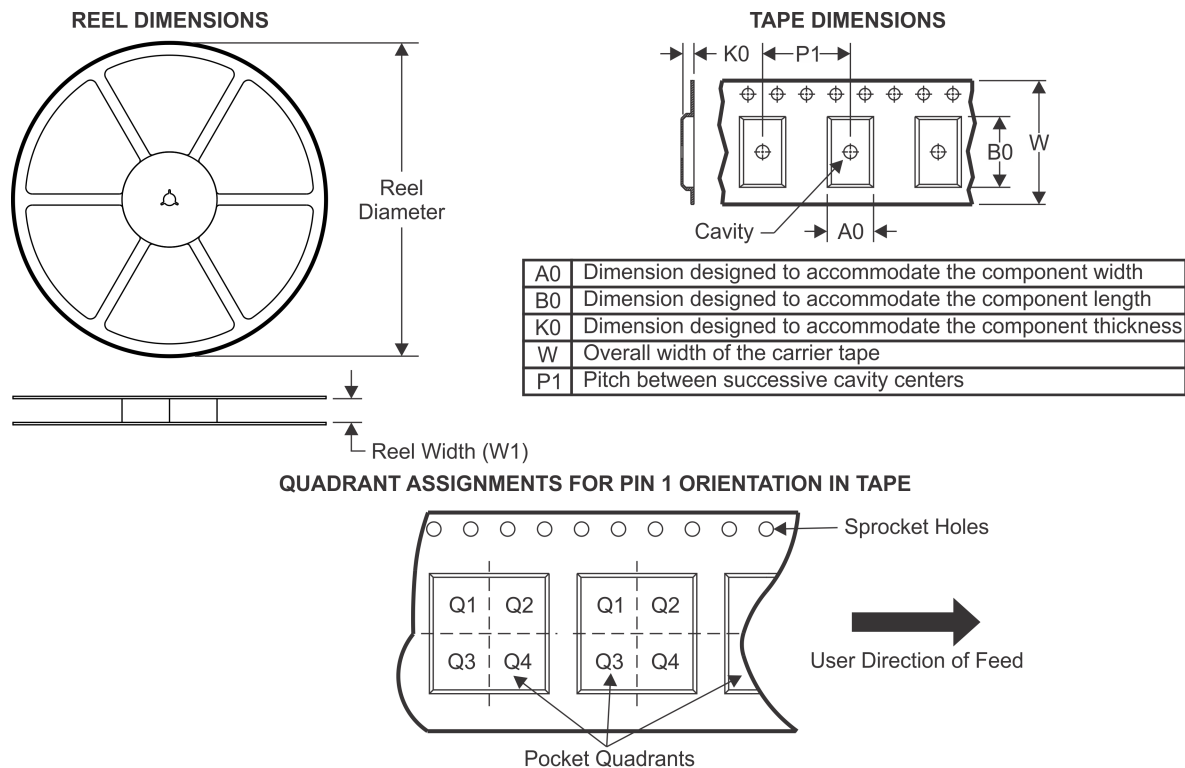
- Changed 300s to 300 μ s in Note 2 of the Abs Max Ratings table [1](#)
 - Changed Q_g Gate Charge Total (4.5V) - max value From: 2.3 To: 12.3 [2](#)
-

Changes from Revision A (October 2009) to Revision B **Page**

- Deleted the Package Marking Information section [8](#)
-

Changes from Revision B (October 2010) to Revision C **Page**

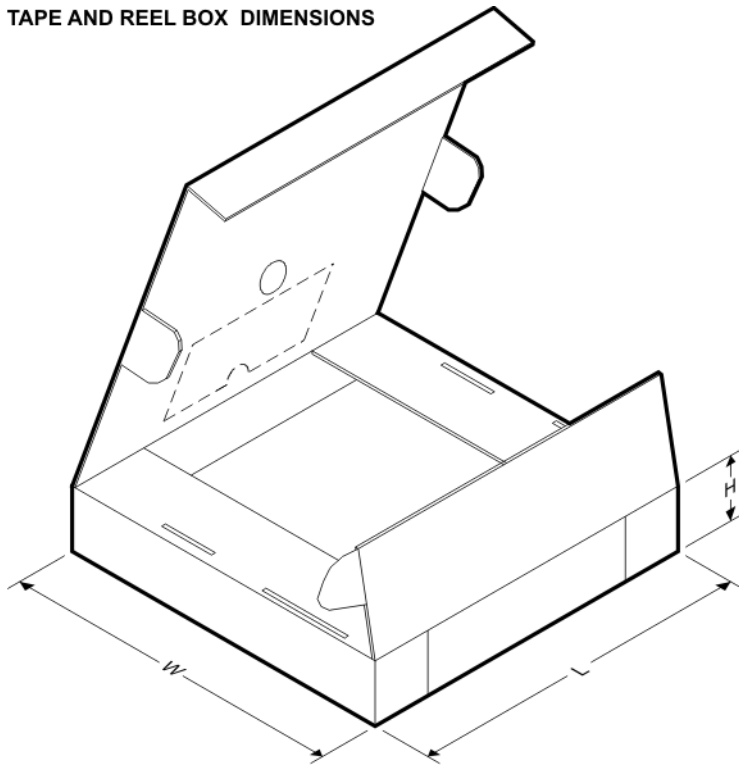
- Replaced the THERMAL CHARACTERISTICS table with the new Thermal Information Table [2](#)
 - Changed the CSD25401Q3 Package Dimensions section [6](#)
 - Changed the Recommended PCB Pattern section [7](#)
-

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25401Q3	VSON-CLIP	DQG	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q1
CSD25401Q3	VSON-CLIP	DQG	8	2500	330.0	12.8	3.6	3.6	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25401Q3	VSON-CLIP	DQG	8	2500	336.6	336.6	41.3
CSD25401Q3	VSON-CLIP	DQG	8	2500	335.0	335.0	32.0

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